AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Listing of Claims:

1.(Cancelled)

2.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 wherein each of the *n* discrete amplifiers comprises a constant envelope amplifier.

3.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 wherein each of the *n* modulators comprises a continuous phase modulator.

4.(Currently Amended) The power synthesizer of ~~claim 3~~ claim 10 wherein each of the *n* modulators comprises a pulse-amplitude modulator.

5.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 further comprising a power combiner having parallel inputs coupled to outputs of the *n* discrete amplitude amplifiers.

6.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10, wherein for each of the *n* stages, the discrete amplitude amplifier has an input that is directly coupled to an output of the modulator.

7.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 further comprising ~~a~~ the discrete amplitude generator having parallel outputs coupled to inputs of the *n* stages~~, said discrete amplitude generator adapted to convert a real input to parallel binary outputs~~.

8.(Cancelled)

9.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10, wherein each of the n stages has an output coupled to an input of a separate transmit antenna.

10.(Currently Amended) ~~The power synthesizer of claim 1~~ A power synthesizer comprising a plurality of n stages in parallel with one another, wherein n is an integer at least equal to two, each of the n stages comprising:

a modulator and a discrete amplitude amplifier in series with one another,

each n^{th} discrete amplitude amplifier configured to apply a gain that is unique as compared to all other of the discrete amplitude amplifiers; and

an actuator configured to simultaneously switch the n modulators, wherein

each of the modulators is coupled to a common actuator~~;~~, and

each n^{th} amplifier is ~~adapted~~ configured to output a signal amplitude $a_0 / 2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said amplifiers~~,~~;

the power synthesizer further comprising a discrete amplitude generator ~~adapted~~ configured to convert a real valued input to a first and second parallel binary outputs that are each coupled to an input of the respective n^{th} modulator.

11.(Currently Amended) ~~The power synthesizer of claim 1~~ A power synthesizer comprising a plurality of n stages in parallel with one another, wherein n is an integer at least equal to two, each of the n stages comprising:

a modulator and a discrete amplitude amplifier in series with one another,

each n^{th} discrete amplitude amplifier configured to apply a gain that is unique as compared to all other of the discrete amplitude amplifiers; and

an actuator configured to simultaneously switch the n modulators, wherein, in one stage, the discrete amplitude amplifier comprises x FETs each having a drain and a gate, and in another stage, the discrete amplitude amplifier comprises $x/2$ FETs each having a drain and a gate, wherein x is an integer greater than two, wherein the x FETs of the discrete amplitude

amplifier of the one stage have coupled in parallel one of gates and drains, and wherein the *x*/2 FETs of the discrete amplifier of the another stage have coupled in parallel one of gates and drains.

12.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 disposed within a mobile station, further comprising an inverse fast fourier transform IFFT block, said IFFT block ~~adapted~~ configured to convert an amplitude modulated input to a bit modulated output.

13.(Cancelled)

14.(Currently Amended) The apparatus of ~~claim 13~~ claim 38, further comprising an absence of a digital to analog converter disposed between the parallel to serial converter and the power synthesizer block.

15.(Currently Amended) The apparatus of ~~claim 13~~ claim 38, wherein each of the at least two discrete amplifier stages comprises a discrete amplitude amplifier and a modulator in series with one another.

16.(Previously Presented) The apparatus of claim 15, further comprising an inverse fast fourier transform IFFT block disposed between the serial to parallel converter and the parallel to serial converter, the power synthesizer block further comprising a discrete amplitude generator configured to convert a real valued input from the IFFT block to parallel binary outputs, each parallel binary output coupled to an input of a modulator.

17.(Currently Amended) The apparatus of ~~claim 15~~ claim 38, wherein the power synthesizer block further ~~comprising~~ comprises at least one power combiner configured to couple an output of each of the at least two discrete amplifier stages with at least one transmit antenna.

18.(Currently Amended) The apparatus of ~~claim 15~~ claim 38, wherein each of the

modulators comprises a continuous phase modulator.

19.(Currently Amended) The apparatus of ~~claim 15~~ claim 38, wherein each of the discrete amplifiers comprises a constant envelope amplifier.

20.(Previously Presented) The apparatus of claim 17, wherein the at least one transmit antenna comprises a first and a second transmit antenna, wherein an output of one of the at least two discrete amplifier stages is coupled to an input of the first transmit antenna and an output of another of the at least two discrete amplifier stages is coupled to an input of the second transmit antenna.

21.(Previously Presented) The apparatus of claim 20, wherein the at least two transmit antennas comprise *n* transmit antennas and the at least two discrete amplifier stages comprise *n* discrete amplifier stages, wherein each n^{th} transmit antenna is coupled to an output of an n^{th} discrete amplifier stage.

22.(Currently Amended) The apparatus of ~~claim 15~~ claim 38~~, wherein the transmitter is~~ disposed within a mobile station or a base station.

23.(Cancelled)

24.(Currently Amended) The method of ~~claim 23~~ claim 40, wherein combining all amplified and phase controlled bits comprises simultaneously transmitting at least two separately amplified and phase controlled bits by separate transmit antennas.

25.(Currently Amended) The method of ~~claim 23~~ claim 40, wherein controlling a phase of the input bit comprises spectrally shaping the input bit with a continuous phase modulator.

26.(Original) The method of claim 25 wherein the modulator comprises a pulse amplitude modulator.

27.(Original) The method of claim 25 wherein the modulator approximately performs Gaussian minimum shift keying.

28.(Original) The method of claim 25 further comprising, previous to providing a separate bit of a bit stream, converting an amplitude modulated signal to the bit stream.

29.(Currently Amended) The method of ~~claim 23~~ claim 40, wherein combining the amplified phase controlled bits in a circuit manner comprises combining all of the *n* amplified and phase controlled bits with at least one power combiner prior to transmission.

30.(Currently Amended) The power synthesizer of ~~claim 1~~ claim 10 wherein each of the ~~*n*~~ n^{th} discrete ~~power~~ amplitude amplifiers apply a gain that differs from that applied by another nearest-power discrete ~~power~~ amplitude amplifier by a fixed amount.

31.(Previously Presented) The power synthesizer of claim 30 wherein the fixed amount is about 6 dB.

32. (Currently Amended) The apparatus of ~~claim 13~~ claim 38, wherein each discrete amplitude amplifier is ~~adapted~~ configured to apply a gain that differs by a fixed amount from that applied by its nearest-gain neighbor amplitude amplifier.

33. (Previously Presented) The apparatus of claim 32, wherein the fixed amount is about 6 dB.

34.(Currently Amended) The method of ~~claim 23~~ claim 40, wherein amplifying a power of the input bit at a power that is unique respecting all other *n* parallel inputs comprises, for each of the *n* parallel inputs, amplifying with a power that differs by a fixed amount from a next nearest power amplification.

35.(Previously Presented) The method of claim 34, wherein the fixed amount is about 6 dB.

36.-37. (Cancelled)

38. (Currently Amended) ~~The apparatus of claim 13~~ An apparatus comprising, in series: an encoder, a serial to parallel converter, a parallel to serial converter configured to output a digital signal at baseband, the apparatus further comprising:

a power synthesizer block comprising at least two discrete amplifier stages in parallel, each stage disposed between the parallel to serial converter, and each discrete amplifier stage comprises a discrete amplitude amplifier configured to apply a gain that differs from that applied by each other discrete amplitude amplifier, wherein each of the stages comprises an n^{th} stage and each n^{th} stage comprises a modulator,

each of the modulators is ~~coupled~~ connected to a common actuator; and

each of the n^{th} discrete amplitude amplifiers is configured to output a signal amplitude $a_0 / 2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said n discrete amplitude amplifiers, and where

the power synthesizer block further ~~comprising~~ comprises a discrete amplitude generator configured to convert a real valued input to n parallel binary outputs that are each coupled to an input of the n^{th} modulator.

39. (Currently Amended) The apparatus of ~~claim 13~~ claim 38 wherein, in one stage, the discrete amplitude amplifier comprises x FETs each having a drain and a gate, and in another stage, the discrete amplitude amplifier comprises $x/2$ FETs each having a drain and a gate, wherein x is an integer greater than two, wherein the x FETs of the discrete amplitude amplifier of the one stage have coupled in parallel one of gates and drains, and wherein the $x/2$ FETs of the discrete amplifier of the another stage have coupled in parallel one of gates and drains.

40.(Currently Amended) ~~The method of claim 23~~ A method comprising:

providing a separate bit of a bit stream on each of n parallel inputs each bit of the bit stream representing a different significance;

for each of the n parallel inputs, controlling a phase of the input bit and amplifying by an n^{th} discrete amplitude amplifier a power of the input bit at a power that is unique respecting all other n parallel inputs;

combining all n phase controlled and amplified bits in one of a spatial manner and a circuit manner, wherein controlling a phase of each of the n parallel inputs is by a common actuator; and each n^{th} discrete amplitude amplifier is adapted to output a signal amplitude $a_0/2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said amplifiers~~,~~; and

~~the method further comprising~~ converting a real valued input to the n parallel input bit streams.

41.(Currently Amended) ~~The method of claim 23 wherein,~~ A method comprising:

providing a separate bit of a bit stream on each of n parallel inputs each bit of the bit stream representing a different significance;

for each of the n parallel inputs, controlling a phase of the input bit and amplifying by an n^{th} discrete amplitude amplifier a power of the input bit at a power that is unique respecting all other n parallel inputs; and

combining all n phase controlled and amplified bits in one of a spatial manner and a circuit manner, wherein, in one of the n discrete amplitude amplifiers comprises x FETs each having a drain and a gate, and an other of the n discrete amplitude amplifiers comprises $x/2$ FETs each having a drain and a gate, wherein x is an integer greater than two, wherein the x FETs of the one of the n discrete amplitude amplifiers have coupled in parallel one of gates and drains, and wherein the $x/2$ FETs of the other of the n discrete amplitude amplifiers have coupled in parallel one of gates and drains.

42. (Currently Amended) The apparatus of ~~claim 13~~ claim 38 comprising at least one transmit antenna.